REMARKS

This is in response to the Office Action dated June 17, 2004. The Office Action rejects claims 1, 14, 17 and 18 over prior art and indicates that remaining claims present allowable subject matter. Applicant amends the specification to correct a typographical error. Claim 1 is amended to clarify its subject matter. Reexamination and early favorable consideration are requested.

The present invention relates to a MOSFET that might be used in the output stage of an integrated circuit. The MOSFET described in the application is formed on a silicon on insulator (SOI) substrate and, as shown in exemplary FIG. 1, has an n-type drain layer 6 that extends from the surface of the p-type active layer 3 to the surface of the buried insulating layer 2. This configuration limits the area of the pn junction between the p-type active layer 3 and the n-type drain layer 6 and so limits the output capacitance of the MOSFET. This advantage is described at page 4, line 30 to page 5, line 1 of the application. As is described through the rest of page 5 of the application, it is possible to achieve not only the desired reduced output capacitance but also a suitable withstand voltage using this configuration.

Independent claim 1, the sole independent claim pending in this application, reflects this aspect of the application's device by reciting, "a second-conductivity-type third semiconductor region formed in said first semiconductor layer *from the surface of said first semiconductor layer to the surface of said insulating layer* ..." (emphasis added). As discussed below, this aspect of the claimed invention is neither described nor suggested by the prior art cited against the pending claims.

The Office Action rejects claims 1, 14, 17 and 18 over Japanese patent publication 07-086,580 (the Hideyuki reference) taken in view of U.S. patent publication 2004/0108544 (the Hossain reference). Applicant submits that neither of these references describes a silicon on insulator (SOI) device in which the second

and third semiconductor regions extend from the surface of the first semiconductor region to the surface of the buried insulator layer, as required by independent claim 1 and its dependent claims 14, 17 and 18.

The Hideyuki reference describes a high-voltage semiconductor SOI device having a buried insulator layer 2 and a first semiconductor layer 3. The Hideyuki reference's device has a p-type layer 4a and an n-type offset layer 7 (second and third semiconductor regions, respectively) formed in a p-type layer 3 (first semiconductor region). Neither of the p-type layer 4a nor the n-type offset layer 7 touches the buried insulator layer 2. This configuration gives the Hideyuki reference's device a high withstand voltage but the fact that the n-type layer 7 does not reach the buried insulator layer 2 means that the junction between n-type layer 7 and p-type layer 3 is large and the device has a high output capacitance. This may cause the device to switch more slowly, which is undesirable in some applications.

By contrast, the device defined by claim 1 requires second and third semiconductor layers that extend from the surface of the first semiconductor layer to the buried insulating layer through the following language:

> "a first-conductivity-type second semiconductor region formed in said first semiconductor layer from a surface of said first semiconductor layer to a surface of said insulating layer, ...;
>
> a second-conductivity-type third semiconductor region formed in said first semiconductor layer from the surface of said first semiconductor layer to the surface of said insulating layer ...."

As plainly illustrated in FIGS. 1-4 of the Hideyuki reference, only the first semiconductor region 3 extends to the surface of the insulating layer. Neither

region 4a nor region 7 extend to the surface of the insulator layer 2. As such, the Hideyuki reference does not meet at least these limitations of claim 1.

The Hossain reference does not suggest modifying the Hideyuki reference's teaching so that the resulting device would meet the limitations of claim 1. The Hossain reference does not describe an SOI device and so cannot teach extending the Hideyuki reference's regions 4a and 7 to touch the buried insulator layer 2.

Nor would it be obvious to modify the configuration of the Hideyuki reference's device to produce the device of claim 1. Modifying the Hideyuki reference's device so that its regions 4a and 7 extend to the buried insulator layer 2 would reduce the withstand voltage of the device, which is contrary to the stated purpose of the Hideyuki reference. Consequently, claim 1 distinguishes over the teachings of the Hideyuki reference taken in view of the Hossain reference and the other references of record. Claim 1's dependent claims including claims 14, 17 and 18 similarly distinguish over the art of record.

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6700 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
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